BACKGROUND HUM

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY BOMBAY
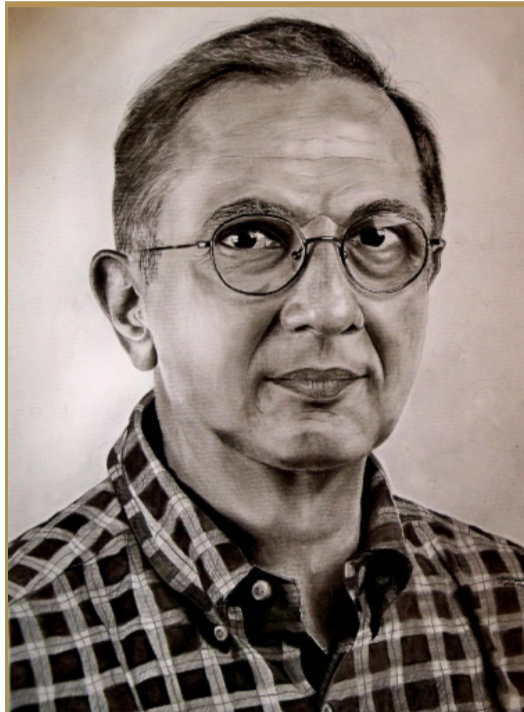
tête-à-tête with Prof. Vasi
TEAM BH

Having completed his Bachelors degree at IIT Bombay in 1969, Prof J. Vasi joined The Johns Hopkins University, Baltimore, USA for his Ph.D. He was a visiting professor at The Johns Hopkins University from 1973-1974. He served as a faculty at the IIT Delhi for 7 years from 1974 to 1981, before joining IIT Bombay as an Assistant Professor in the Department of Electrical Engineering in 1981.

Here, at IIT Bombay, Prof. Vasi is the Principal Investigator for the NCPRE (National Centre for Photovoltaic Research and Education), set up by the govt. of India, that works on solar cells and grids. He is now retired, and an emeritus professor.

One image that every student who was a freshman here, will recount with longing is of Prof. Vasi, serenely walking into the EE112 class, with that mug of coffee and as cool as a cucumber. One can't help but be reminded of Dumbledore.

SKETCH BY SHREYANS GANDHI

BH: Sir, What was our department back then when you set foot as a young faculty?

Our department was good academically and professionally strong. It thrived on the ethos of an open atmosphere, encouraging ideas and discussion. The Faculty were approachable, and it was the tradition of EE department to be open. As a young faculty here, I was given enough space for ideas, and frank discussions, which impressed me a lot. We still continue with that tradition, and encourage our new faculty who are the future of our department.

BH: Our readers would be grateful to hear your perspective on the changes that have swept across our department over your distinguished career?

During the 80's we realized that we needed to focus more on creation and dissemination of knowledge, instead of only dissemination of knowledge through teaching. There has been a sea change in the research infrastructure and an increasing populace of PG students, along with research oriented faculty has driven the research in our department since 80's. The research funding scenario has improved dramatically since then. Newer research and teaching labs have come up. Our nanofabrication facility is probably one among the top five to eight such facilities in the world.

BH: Where do we stand when compared to foreign universities?

We have made enormous strides in the last 20-30 years. In the 1980's, many American and European universities were way ahead of us. Now we rank reasonably high, and have an "equal" relationship with many international universities. However, a thing of some concern is that though we have improved, universities from many other countries, such as China, Brazil, Korea, which were nowhere in the picture 25 years ago, have progressed very fast and some of them are now ahead of us. However, I am very optimistic that the level of R&D activities at IIT Bombay and other leading places in India will continue to improve dramatically, and it is not impossible that work done in India can well set the research agenda which will be important for many other countries also.

BH: What is your philosophy towards teaching and grading?

Most important thing is to get a student interested in a subject. You cannot teach a student everything he/she needs to know. About grading, I'm a fairly liberal grader. On the other hand, you won't have half of my class getting an AA. If someone really does badly, they get an FR. If a student has done reasonably well, it is advisable, to encourage them. They have a lifetime of learning ahead.

"The department should embrace both research and teaching."

BH: What is your take on students losing focus on research and taking on careers in various other sectors, for example financial sector?

I don't think there has been a huge shift. This modulation has been a result of what has been going around in the outside world. I cannot say that there has been a monotonic dramatic shift. There were always students who wanted to do management, and entrepreneurial activities. Lots from my batch did it. Not all of them were related to EE. 5-8 years ago, there was a lot more interest in financial jobs, but it has also decreased now. At one point, during the 80's and 90's there was this impression that to get a good career, you had to get a post grad degree. Then you found that students were much more concerned with academics. They had to get good grades.

BH: With the increase in Batch strength, do you see a decrease in student teacher interaction? Would one have asked a doubt that they otherwise would have in a smaller batch?

This is difficult to answer because the strength of classes has changed, but also I have changed. Now I have much lesser time. So, I cannot categorically answer this. A batch of 50-60, for me is almost same as 120. Across the table discussions are almost impossible for batches of even 50 students.

BH: Where do you see our department going to in the coming few years?

It should embrace both research and teaching. Only research, then it'll become esoteric, and we won't have the next generation of researchers. If only teaching, then it won't excite students, or we won't be able to pass on our passion or enthusiasm to them. Research must be accessible to everyone, including undergraduates.

CONTENTS

CONFESSIONS OF A RESEARCH SCHOLAR
VANDANA

Vandana is a Ph.D from the power electronics section of the department. She is passing out this year, after submitting her thesis. She has been here for 6 years (Mtech + Ph.D) . Here is a small writeup from her, about the department.

I first came to IIT bombay in the monsoon of 2006. I had then just finished my undergraduate studies. I expected something quite out of this world and when I came here, the scales did not fall from my eyes. I got the BE degree from a college where people come more to socialize than work , and not being a particularly social sort, I did quite well in my studies .Indeed, I was considered quite smart. I thought I was pretty smart too…that is, until I came here.

Professors were fond of saying: "You are here because you know nothing" and " You first have to unlearn everything you studied in the last 4 years. " It is quite funny to think that I found all this rather insulting then. Initially, each day made me realize in a new way : I do not know anything. After the first week, I wanted to leave. There seemed to be a lot of positives in quitting the program returning home, and helping with the housework. Time passed and I did not want to leave anymore. But I was afraid they would chuck me out for not making the minimum CPI.

The first semester was awfully hectic, I had to take some courses I had hoped to see the last of. Complete with assignments, course projects, all rather difficult for a person who had rarely studied from anything except locally published textbooks.
One course in particular was really hard. The instructor taking the course was brilliant, but rather lacking in patience. We were all intimidated by him, as he seemed to know so much. But he went so fast and lost us somewhere along the way. The blank looks on our faces after he had explained an intricate principle painstakingly would send him into paroxysms of rage. An assignment was due and no one in the class had been able to do it. At the very last minute, someone had an inspiration. Soon, 40 odd identical assignments found their way to the instructor's mailbox. He was more pained than angry.

"What is the problem? Are you not following? "
"No"
"Is it too fast? "
"Yes!"

"Why can't you stop me and ask when you don't understand? "
"Because, I blurted out, we're all rather scared of you."

I do not know what possessed me to say the last sentence. I feel sorry, to this today. It was an inconsiderate thing to say. To my surprise, he was not angry. The next day onwards, he changed became less intimidating, more patient. And I realized the kind of place I had come to.

People at the campus change over time. Take me for instance. When I came, I knew nothing. Show me a circuit, ask me to analyze it, and I would have broken into a cold sweat. I would never have acknowledged that any of my peers were good. It was beneath my dignity to call anyone clever. I could not take criticism. I suppose I was arrogant and ignorant at the same time. Now six years later, I can honestly say, I'm a far better engineer and a much better person. In many ways, this institute shows you your place.

After two years of my Master's degree, I realized that I could not leave. There was so much more I could learn here. Although, there were times I wondered if I was crazy. At times this campus seems like a prison, and you wonder when you will be up for parole.

Now, the time has come (or is coming, you can never tell in a PhD) for me to leave. Do I want to? Yes and no. I see my friends, they have moved on with their lives, they have families, jobs ... I suppose I want those too someday. They love asking you this question in personality tests : Are you happy when a task is finished or when it is starting? I'd go with the latter. It means there's nothing more you can do. You look it over and think, is that all? Sometimes I feel jealous of the students who are just starting.

There are some people here I can't imagine my life without. I dread the day I will make my last visit to the lab, my last walk down the Infinite Corridor. Still, I can't stay here indefinitely. The "What, you're still here" will become even more frequent. I will be shown to visitors to the department: "This research scholar has been here for the last x years."

I guess, the bottom-line is : I must leave, and move on with my life - But this is not goodbye, shall we say,
Au revoir?

"Elec junt a ho, mugg lo".
RITIKA BHAMARE

Freshman year! Ah, it begins with all the yelling through infinite orientations that go on until midnight and you're hardly aware of the number of assignments and quizzes you have lined up for the next week.

'Vidyut Abhiyantriki Vibhag' (the sophomores liked our calling it that, I believe!), the only department with two DIC's in the first year. EE 111. The maverick of a course responsible for making us sit through quizzes on Saturday mornings or keeping us up late on Wednesday nights. Cramping us into one room writing assignments to be submitted the next day (Exception being the first one or two assignments that were solved individually and in advance!). As the semester proceeded, neither does the course get any easier nor do we get any better. With lectures late in the evening, leaving us with very little time to study for other courses, we mass bunk only to be dragged to the department head who is all the more infuriated by people coolly walking in half an hour late!

Another course, IC 102. The professor, a man strongly opposed to partial marking for reasons unknown but having an amazing sense of humour, which mostly went unappreciated! Lectures started two weeks late, that too with statistics and basic probability and we wondered why there was such a fuss about this course! But in almost no time stuff scraped right off our heads while we had surprise quizzes being tossed at us from all angles. So by the time the mid-semester exams closed in on us, we began to realize the importance of "those six hours a week" we constantly heard about.

Yet, in spite of all the drowsy mornings through these classes in LCH 11, today, the mood is certainly enchanting with the department orientation being held here. The boys introduce themselves to the seniors in 'shudh hindi' and sing and dance and do whatever they're asked for. While the girls, who were initially a little awkward to say or do anything considering the skewed sex-ratio, eventually become a part of the whole thing as the mood lightens. We start to enjoy this. We enjoy being here.

Academia may be a roller-coaster ride for us, but as we walk through the infi corridor there is a sense of belonging whenever we look at the four buildings of the electrical engineering department. The feeling of pride which accompanies when we triumphantly end a conversation with a non-elec friend saying, "hum toh elec wale hain!" is overwhelming. Now, with a whole semester behind us, it hardly feels like any time has past. But we are all settled now and it feels like home.

In conversation
with
Akshata Athawale
Senior Undergraduate, EE

Akshata, and Prof. Animesh Kumar, have been awarded the best student paper at the SPCOM conference recently held at the Indian Institute of Science Bangalore. In spirit with the Institute's focus on Undergraduate Research within it's broader aim to improve research at IIT Bombay, Background Hum caught up with Akshata to know more about her recent award, her research and how it came about.

It was during late March, that Akshata first thought about getting an intern during the summers. Late march is very late, by any standards, but she managed to crack an intern at Larsen and Toubro, Bangalore. She went to get her "No Objection Certificate" from her facad, Animesh Kumar, who voiced his opinions about her working in the department itself. This seed of a thought, led to Akshata finally working with Prof. Animesh Kumar itself.

*The title of the paper is **"Dithered A2D conversion of multidimenstional smooth non band limited signals".** You can find this on IEEExplore, which is accessible to any computer on the IITB LAN.*

To explain it in simpler terms, consider a rectangular area. Assume it has a temperature distribution, which we would like to find. This temperature is the multi-dimensional signal in question. To estimate the distribution, we would have to put sensors at every point in space, which is not possible. Relying on the fourier transform properties, we would like to estimate the temperature at all points, just by sampling it at a few relevant points. Too many sensors, pushes up cost, while using only a few increases the error. Also, the position and the number of sensors in each dimension (x or y) has to be calculated and optimised.

If this gets you interested, consider reading the original at http://tinyurl.com/av6oran

Prof. Animesh had a clearly defined problem for Akshata to work on. It was an extension to his earlier work on a similar topic. Akshata confesses that initially she was not generally a very research-enthu person, in IITB student lingo. She credits Prof. Animesh for seeing to it that she was interested in the problem, and meeting her regularly to offer his inputs as well. In her words, "(if) there was a definite problem, I had to think about it, formulate a solution, get nice mathematical expressions, and analyse results" (look at the Box, for more details). Over the duration of the summer, she accumulated all her results, and had begun to write a report on the work she had done. Prof. Animesh suggested that she writes a paper on the work done, and present it at a conference, as it would be a new experience.

She spent the third year going about writing the paper, and finally made the deadline of the SPCOM conference. In retrospect, when asked if she regretted not doing an intern abroad, she expressed her inability to compare the two. Adding that, she wouldn't have written this paper and ending up winning the best student paper award at the conference, had she interned elsewhere. She smiles and signs off, time and again we realise Frost's words:

"Two roads diverged in a wood, and I --
I took the one less travelled by,
and that has made all the difference."

Note: This articles reflect the opinions of the writer alone and can only be indicative of those of the writer.

Know thy turf - Centre of Excellence in Nanoelectronics

The Department of Information Technology, Government of India, in a bid to jump into the bandwagon of Nanoelectronics research, established two Centres of Excellence in Nanoelectronics, one at IISc, and the other at IITB, way back in 2006. You could walk into the lab next door, and make your own quantum dot or quantum well structures. Background Hum covers this lab, an intergral part of the Electrical Engineering Department in this edition of know thy turf, with a difference.

Devices that combine mechanical and electrical principles at the microscale. How about structures that pick up vibrations to convert them into energy?

High Electron Mobility Tranistor, III-V detectors!

Bio MEMS

Impacts areas like homeland security and public health. Devices made can sense heart attacks, and detect TNT

Smallest ever in India

MEMS

What goes on in this lab ?

Carbon Nanotubes and Graphene for electronic Applications

Yes, those length scales at which quantum mechanical effects set in

A sub-100 nanometer transistor!

Tunnel Field Effect Transistors

IITB

Novel Material based

Better, faster storage devices at the end of the day

Solar Photovoltaics

Memory devices such as metal-nanocrystal flash, resistive RAM and spin transfer torque-RAM

Who are the Stakeholders ?

The Government of India

Silicon   Si

The Oxide

The patterning

INUP Making Nanoelectronics accessible to anyone. Any student from other colleges in India can work at CEN, after prior approval

Furnaces for growth of oxides, and deposition of various other materials like poly-Si and Silicon Nitride

Lithography tools

Pattern Silicon. Choose selectively which area you would like to modify

Characterisation To check if what you have done, has come out the way it was intended to

Cool stuff the Lab can boast of !

Applied Materials

Implantation, Molecular beam epitaxy, electron beam evaporation

Getting doped regions in + Metals

Has a partnership with IIT Bombay. There is a an Applied Materials lab with state of the art Instruments

Wire Bonder

Take contacts out, interfaces silicon with the outer

Take wires out

SPEECH TRAINING SYSTEM FOR HEARING-IMPAIRED

Ever heard yourself speak while having your earphones on, and been shushed by your friends ? Now imagine a person who is born deaf trying to speak. The lack of auditory feedback is a major reason for speech disability. Prof. Pandey's lab makes aids that enable speech, by providing alternate methods of feedback for the deaf.

Children with normal hearing capabilities acquire speech readily during the first few years of life. They use auditory feedback for speech correction. Auditory feedback during speech production is believed to play a critical role by providing the nervous system with information about speech outcomes. This is used to learn and subsequently fine-tune speech motor output. The development of speech in children with early hearing loss is often disrupted due to lack of auditory feedback. Children with hearing impairment have great difficulty in acquiring the ability to control position and movements of various articulators (lips, tongue, vocal chords). Some of the articulation errors include confusion of the voiced (eg: /g/) and voiceless sounds (eg: /k/), added nasality, misarticulation of the consonant blends, substitution of one phoneme (basic unit of language's phonology) to another, omission of consonants at the beginning and end of a word (eg: omission of /p/ sound in /pack/) etc. Thus, children with hearing impairment are generally not able to produce intelligible speech, despite having proper speech production mechanism. However, oral communication skills are important to children with such disabilities as these can influence the utilization of social, educational, and career opportunities available to them. Hence, 'speech training', which can enable the hearing-impaired children to produce intelligible speech, is essential.

It is possible to teach deaf persons to speak by using an appropriate non-auditory feedback like a tactile or visual feedback, which can be used to provide the required information. Advances in processing and analysis techniques in speech science, electrical engineering and computer science have increased our knowledge of normal speech production. In turn, these technological advances have been applied to the development of clinical assessment and training procedures for hearing-impaired children. Visual feedback can be provided by a display of acoustic and articulatory speech parameters related to articulatory efforts which are easily controllable by the person undergoing the speech training. Speech intensity, pitch, spectrogram, vocal tract shape, lip shape, and consonantal features like voicing and nasality have been used for providing visual feedback via speech training aids.

It has generally been agreed that phonemes produced in the front of the mouth are more often produced correctly than are the phonemes produced in the back of the mouth. Thus, bilabial i.e. articulated with both lips, consonants (Eg: /b/ and /p/) produced by hearing-impaired persons tend to be more intelligible than lingual consonants (Eg: /k/ and /g/) and vowels (Eg: /a/ and /i/). This makes sense when one considers that the relative visibility of articulatory gestures should be important to hearing-impaired persons while learning the production of specific sounds. Based on this fact, speech training aids which provide visual feedback of the vocal tract (cavity from lips to glottis) shape were used for speech training of vowels. These training aids were found to be useful for improvement of vowel articulation. In such training aids, the vocal tract's shape during the vowels articulation are estimated using linear predictive coding (LPC) analysis of speech. Linear predictive coding is a tool used mostly in audio signal processing and speech processing for representing the spectral envelope of a digital signal of speech uncompressed form, using the information of a linear predictive model.

Vocal tract shape is the area of cross-section at each position in vocal tract. Its estimation using LPC fails during stop closures due to low energy and lack of spectral information. Currently, there are no speech training aids in the market for teaching the articulation of stop consonants using visual feedback of the vocal tract shape. Hence, a technique for accurately estimating the place of articulation of stop consonants (a consonant in which the vocal tract is blocked so that all airflow ceases. The occlusion may be done with the tongue (blade [t], [d], or body [k], [ ]), lips ([b], [p]), or glottis) is needed for improving the effectiveness of speech-training

aids. In our lab, a method has been developed to estimate the vocal tract shape during the stop closures of vowel-consonant-vowel (VCV) utterances by performing interpolation of bivariate polynomials based on estimated area values during VC and CV transition segments in VCV utterances.

We have developed a prototype of the speech training aid for teaching the vowels and consonant articulation. The speech training aid consists of a slow moving animation to display the vocal tract shape, pitch contour, spectrogram and other speech parameters. The speech parameters of reference or teacher and the hearing-impaired children are displayed side by side to help the children to match the articulation with respect to the target.

The estimation of vocal tract shape from speech signal recorded from the microphone involves relating the model used in LPC analysis of the speech signal to an acoustic tube model of the vocal tract. Vocal tract is modeled as a lossless acoustic tube with sections of equal length and varying cross-section area (acoustic model) and also as an all-pole filter (LPC model). We can abstract from its curvature and divide it into cylindrical sections of equal width. Depending on the shape of the acoustic tube (mainly influenced by tongue position), a sound wave travelling through it will be reflected in a certain way so that interferences will generate resonances at certain frequencies. These resonances are called formants . Their location largely determines the speech sound that is heard.

Reflection coefficients (ratio of volume velocities at section interfaces) are obtained from LPC analysis of speech signal. A reference area is required for determining vocal tract parameters. For improving the estimation, the lip opening area estimated from a video recording of the speaker's face is used as reference area. A technique for estimating the area of the lip opening based on template matching is currently being investigated. An example of the lip opening estimation using the elliptical templates is shown in figure. Read more on http://www.ee.iitb.ac.in/~spilab/papers/2012/paper_nsnayak_ncc2012.pdf

Our current system helps in correcting the place of articulation of consonants but feedback for correcting the manner
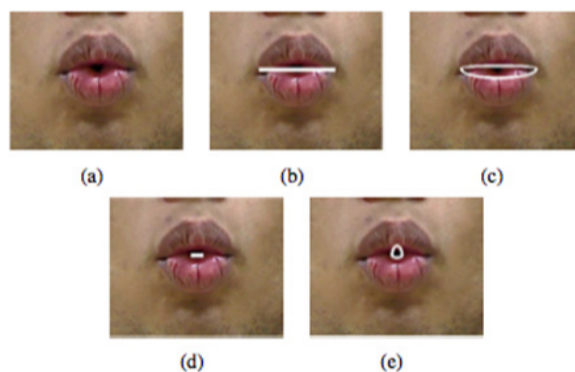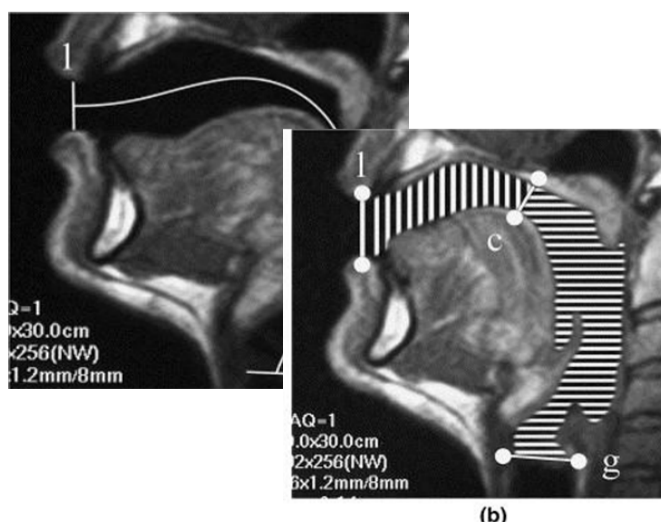
Figure 9. Lip opening estimation for /u/ : (a) original image, (b) horizontal strip template fitting, (c) filled ellipse fitting (incorrect), (d) horizontal strip template fitting (corrected), and (e) filled ellipse template fitting using corrected horizontal strip as major axis.

of articulation like timing and coordination still need to be addressed. There is a need to develop more intuitive interfaces using video games and animations to make learning faster and more interesting.

Course Wiki
www.tinyurl.com/coursewiki

Begin registration time, before the semester, and everyone runs door to door asking about which courses to take. Some are concerned about the how the grading for a particular course was, while others want to know if the recruiters would look upon this course favourably. The more planned ones would like to know if a course requires any prerequisites.

Sadly, the curriculum page on the Department site is archaic. The course content is nowhere similar what is taught in the class. It has not been updated in a long time. The D-AMP, Department Academic Mentorship Programme, has taken matters into its own hands, by introducing a course wiki. This works on the same principles as Wikipedia, where users contribute course reviews, so that the community can make a more informed choice.

On the course wiki, you can look at the course content, from when the professor last took the course. People who have taken the course, suggest prerequisite courses which help you get the most of the course. Also, one can know which professors have taken this course in the past, and are likely to take it up the future. An approximate measure of the course load is also provided. For the CPI conscious, the grading trend is explained, and finally, in subjective terms, why or why not you should take this course is elaborated.

A course wiki like this thrives on student reviews. All reviews have been contributed voluntarily, for the benefit of the student community. D-AMP would like this opportunity to request everyone to contribute reviews of courses that they have taken especially the 6xx and the 7xx courses.

A TOUR OF VLSI LAB PART II

K. NAVEEN & SIVARAMAKRISHNA

Part I featured the research activities and the projects conducted in the VLSI Lab.

In this part, we walk you through the procedures followed in taking projects from concept to an Integrated Circuit.

Here are the steps delineating the fabrication process:

Architecture level design

A project is kicked off by the selection of a 'target application' and the definition of its specifications. Futuristic applications are generally targeted as they set the bar high for the specifications. A block diagram of the system is then sketched.

The above step is repeated (recursively) with each of the sub-blocks of the system until they become sufficiently simple to be manageable. A literature review for the design of each of the blocks follows. Some systems need System Level Simulations for optimizing the parameters of the system. They use macro-models for the sub-blocks.

Circuit Design

The individual blocks are designed at the transistor level once the system parameters are set. The appropriate application-specific technology is chosen for the system implementation. Commonly targeted applications are high frequency performance, low leakage, radiation resistance and high fidelity.

The SPICE/Spectre models of all the available devices in the designated technology are used in circuit simulations for design optimization.

In scaled technologies, the disparity between the fabricated devices not only manifests among batches and wafers but also dies. The foundry usually throws in a 'mismatch file' with the model file . This file contains data pertinent to the maximum variations that are likely to occur in the technology.

Layout

A layout is a set of "images" which define the various masks that are used to fabricate the design. The layers that are defined by the masks are of metals used for the interconnects, of oxides and silicon which form the active areas (the transistors), and a few other elements which are used for furbishing the transistors for improving the performance especially at shorter technology nodes.

The transistors and other devices are first placed at appropriate positions and then the interconnect is routed using metal layers. More often than not the most compact layout yields the best performance in terms of speed and power.

The layout then needs to be checked for "Design Rule" violations, by a step often called DRC or design rule check. This checks whether the various mask shapes and spacings drawn are manufacturable in the particular technology. Once the DRC is clear, a layout versus schematic check is done to ensure that the layout and the schematic are consistent.

The next step is to extract the parasitics at various nodes that appear due to the interconnect, the transistor layout and the fingering. The extracted netlist (the description of the connectivity of an electronic design) needs to be simulated to verify the performance. Often high frequency circuits take a major hit due to layout parasitics making the design iterative in a loop that includes layout and post layout simulations.

Fabrication Facilities in India

Setting up a semiconductor fabrication facility (which will be referred to as a foundry/fab henceforth) is a 3-4 billion dollar affair. That said, the construction (let alone the operation) of such facilities here at IITB, is at best a reverie.

Several attempts have been made in vain to set up a fabrication facility in Hyderabad in 2006.

The Department of Space administered Semi-Conductor Laboratory at Mohali is planning to upgrade its current 0.8 micrometer technology to produce chips of the 0.18 micrometer technology (22nm is considered state of the art). One of IIT Bombay's main research aims at CEN is to fabricate a 100nm transistor.

Tale of Fabrication

Taiwan and China are leaders in fabs. Taiwan Semiconductor Manufacturing Corporation (TSMC), United Microelectronics Corporation(UMC), Global Foundries, On semiconductors, etc. are some prominent semiconductor foundries. They offer 'Multi-Project-Wafers' (MPW) either by themselves or through mediators like MOSIS, Europractice, etc.

Hundreds of designs (of size 2mmX2mm) from various agencies around the world are clubbed together and fabricated on a single wafer (typical size of a few inches) to reduce fabrication costs. Once fabricated, the wafers are cut (into what are called 'dies') and delivered to the respective customers. These dies are either packaged by the above specified mediators or by third party IC packing companies like SPEL Semiconductor Limited, Tessolve.

Getting the IC fabricated

The project teams congregate and wage a war for the distribution of the silicon real estate for their utility. The designs are put together and re-simulated for verification. Designs are sent for fabrication in the form of a computer readable stream format called Graphic Database System (GDS). The foundry uses these files to generate the masks for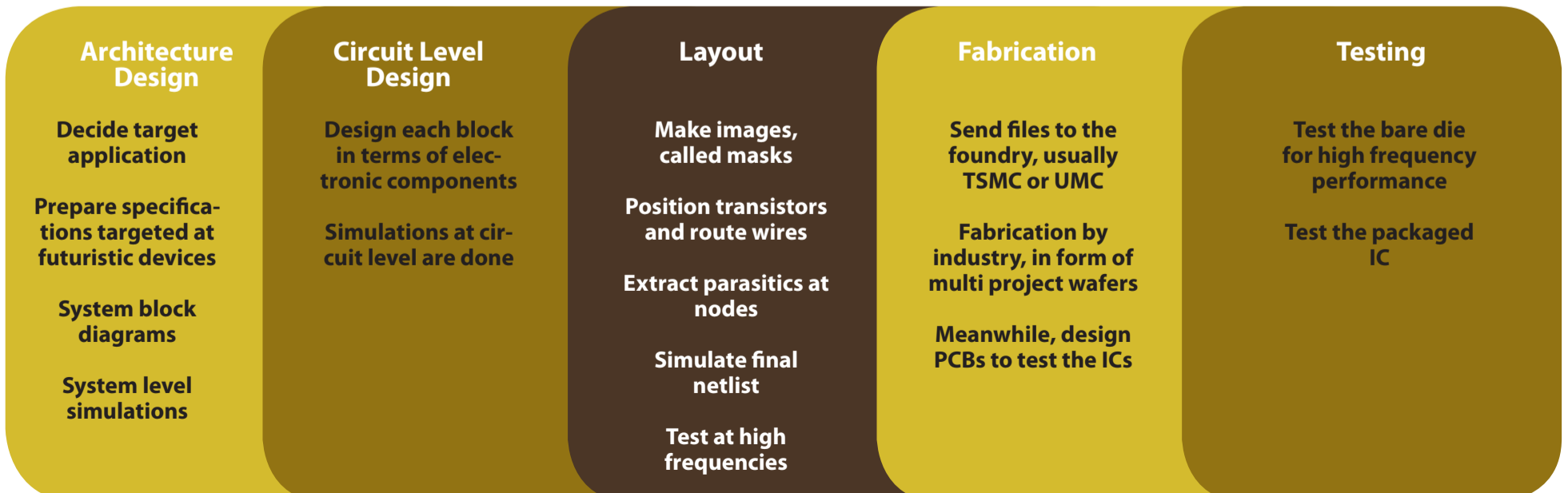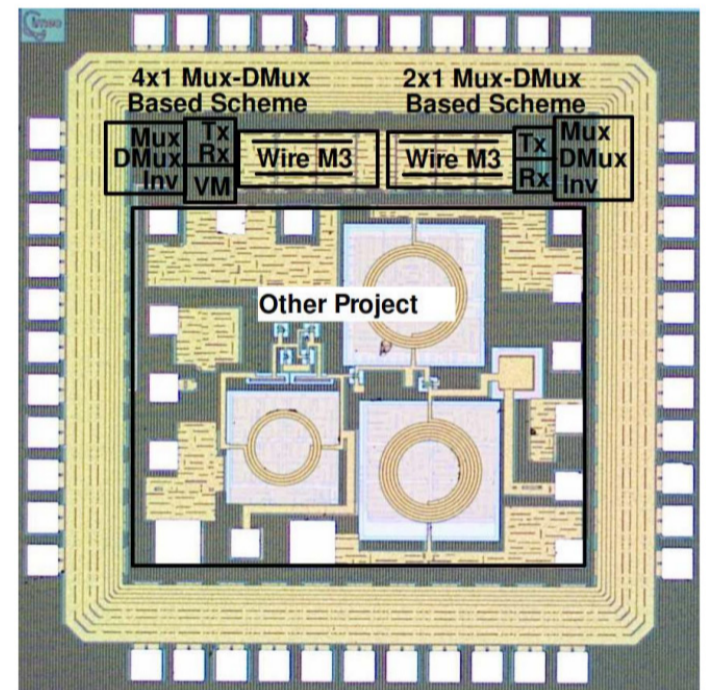 the fabrication. It takes 3 to 4 months to get the fabricated chips. Meanwhile, the students work on strategies and design PCB circuitry to be used later for testing purposes.

Testing

The ICs available in the WEL and other labs are packaged. Inside these dwell the dies - the actual ICs. The dies are packaged in ceramic/plastic containers with pins that bond to the pads on the die. Here's an interesting analogy – the ceramic container is like a cocoon (or chrysalis, maybe?) to the moth that is the die which is encased by it. These packages can then be soldered on boards or mounted on breadboards.

Packaged ICs simplify testing. But they add parasitics which may deteriorate high-frequency performance. ICs meant to operate at high-frequencies, are generally tested without getting them packaged in the first go. This process is known as bare die testing.

These bare dies are mounted on probe-stations and high-frequency input signals are fed through probes that are as thick as an average human hair strand (a few micrometers). High frequency testing a.k.a RF testing equipment consists of a probe station, probes, RF source meter unit, Spectrum Analyzer, RF Network analyzer, etc.

Architecture Design	Circuit Level Design	Layout	Fabrication	Testing
Decide target application	Design each block in terms of electronic components	Make images, called masks	Send files to the foundry, usually TSMC or UMC	Test the bare die for high frequency performance
Prepare specifications targeted at futuristic devices	Simulations at circuit level are done	Position transistors and route wires	Fabrication by industry, in form of multi project wafers	Test the packaged IC
System block diagrams		Extract parasitics at nodes	Meanwhile, design PCBs to test the ICs	
System level simulations		Simulate final netlist		
		Test at high frequencies		

"Gotta Play The Music"

ARJUN RAO

This summer, a group of second year undergraduate students of electrical engineering, A Rao, A Shankar, A Ambhore, won the Institute Technical Summer Project- Best Research Award. The project was about making a prototype of a polyphonic sound generating device (synthesizer) using arduino duemilanove platform(Atmega 328). Background Hum presents you with an insight into the project.

Intention:
The intention of the project was to construct a polyphonic instrument i.e. capable of playing more than one note at a time.
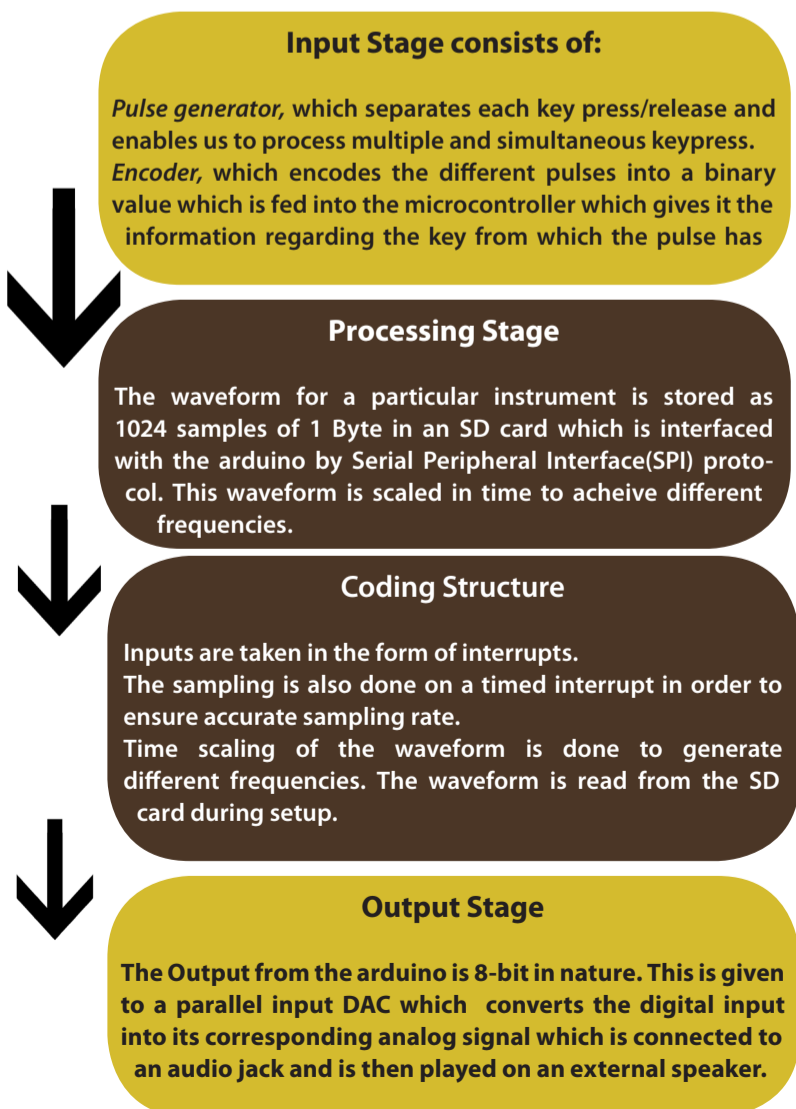
Intended Features:

1. Ability to play multiple notes (as many as can be supported by microcontroller (µC)) simultaneously. thusly, to develop an input system capable of 'theoretically' handling a significant no of simultaneous key-presses (keeping in mind limited input ports of the µC).

2. Ability to create and setup instrument patch in order to hear different instruments.

Realised:

A four key prototype of a polyphonic synthesizer, i.e. a maximum of four notes can be played simultaneously. However, the input system is capable of handling more than 4 simultaneous inputs, the above limitation being due to processor limits. The sample rate achieved is around 25000 Hz which provides a fairly decent sound quality. We have managed to develop sound waveforms (patches) for three instruments (violin, flute, synthetic brass), store these waveforms in the SD Card and program the Arduino to retrieve and use them. Our initial expectation to build more keys failed due to cost and time constraints.

1. Four note polyphony i.e. four notes at max can be played.
2. Achieved the implementation of input system that can handle multiple key-presses.
3. 25000 samples/s sample rate.
4. Creating a basic waveform patch for three instruments violin, flute, and synthetic bass by Fourier analysing MIDI sound samples.
5. Storage and retrieval of patch waveform information from SD card.
6. Basic hardware de-bouncing.

Input Stage consists of:

Pulse generator, which separates each key press/release and enables us to process multiple and simultaneous keypress. *Encoder,* which encodes the different pulses into a binary value which is fed into the microcontroller which gives it the information regarding the key from which the pulse has

Processing Stage

The waveform for a particular instrument is stored as 1024 samples of 1 Byte in an SD card which is interfaced with the arduino by Serial Peripheral Interface(SPI) protocol. This waveform is scaled in time to acheive different frequencies.

Coding Structure

Inputs are taken in the form of interrupts.
The sampling is also done on a timed interrupt in order to ensure accurate sampling rate.
Time scaling of the waveform is done to generate different frequencies. The waveform is read from the SD card during setup.

Output Stage

The Output from the arduino is 8-bit in nature. This is given to a parallel input DAC which converts the digital input into its corresponding analog signal which is connected to an audio jack and is then played on an external speaker.

Resource Allocation

(by Narendra N, Srinivas under the guidance of Prof. Prasanna Chaporkar)

Wireless broadband access is growing in popularity. To sustain the growth, these access technologies have to support and provide required Quality of Service (QoS) to various applications including real-time applications. Moreover, access should be extended over as large as area as possible in a cost effective manner. WiMAX, which is an acronym for Worldwide Interoperability for Microwave access, is one of the promising technologies which can be used to sustain the growth. The key challenge in WiMAX is then to design a resource allocation scheme that provides the required QoS to each service class.

Currently, WiMAX characterizes applications into four classes, viz.

1. Unsolicited grant Service (UGS): supports the constant bitrate (CBR) applications like VoIP that require low latency and low delay jitter.
2. Real-time Polling Service (rtPS): caters to the Constant Bit Rate (CBR) traffic with variable packet size, e.g. MPEG video.
3. Non-real-time Polling Service (nrtPS): used for delay tolerant services that require minimum rate like FTP and HTTP.
4. Best Effort (BE) service: used for services that do not require any minimum rate.

WiMAX standard has evolved over time from 802.16d supporting single hop, stationary users to 802.16e supporting single hop, mobile users and further to 802.16j supporting multi-hop, mobile users. WiMAX uses a multiple access technique called Orthogonal Frequency Division Multiple Access (OFDMA) which combats Inter Symbol Interference (ISI) and fading.

Throughput (bits transmitted successfully per frame) and fairness (a metric used to measure the distribution of resources among the users) are the two important factors to be considered when designing a resource allocation scheme. There is a trade off between throughput and fairness. For example, a resource allocation scheme that provides resources to user based on high Signal to Interference plus Noise Ratio (SINR) provides higher throughput but poor fairness. Also, fairness schemes like max-min fairness allocate most of the resources to low SINR users thereby reducing network throughput.

To cope with this trade off, we have come up with a resource allocation scheme based on the concept of time fairness i.e. our scheme allocates equal number of slots to each user in a frame while taking channel conditions into consideration. The key challenge in this scheduling scheme was:
a)   determining the number of slots to be allocated to each user
b)   determining which slots to be allocated to each user.

To solve these, the resource allocation problem was mapped to a maximum weighted matching problem in bipartite graphs.

Proposed Algorithm:
Resource allocation of OFDMA slots is a two dimensional problem. This is because, each user can transmit at different rates for same frequency and time slot depending on their channel condition. For example, consider the figure below

USER 1(X)	Time slot 1	Time slot 2
Frequency 1	X11	X12
Frequency 2	X21	X22

USER 2(Y)	Time slot 1	Time slot 2
Frequency 1	Y11	Y12
Frequency 2	Y21	Y22

User 1 can transmit at data rates given by Xij, in the respective frequency and time slot. So can user 2 with data rates given by Yij. However, only one user can be allotted a particular frequency and time slot. Hence, it is a two dimensional problem. The challenge is to select which slot to be given to which user so that the throughput is maximized. To solve this, the two dimensional resource allocation of OFDMA slots is converted to a single dimensional resource allocation problem as shown in figure 2.

User 1	X11	X12	X21	X22
User 2	Y11	Y12	Y21	Y22

Since there are two users, I need to assign 2 slots to each user as per our idea of slot fairness. This single dimensional resource allocation problem is solved by using maximum weighted matching in bipartite graphs.

Maximum Weighted Matching can be used in assignment problems. Consider an assignment problem, where there are N persons and N jobs with each person having different skills for various jobs. Each person can do a single job and each job can be assigned to only one person. The cost matrix can be represented by NXN matrix with each element representing a profit (pij ≥ 0) incurred by assigning a jth job to a ith person. The aim is to assign each user with a job such that the total profit gained by this assignment is maximized.

However, assignment problem requires us to have a square matrix. But, if we have 2 users and 4 slots which need to be assigned, we end up having a 2X4 matrix which cannot be used in assignment problems. Since we use slot fairness, we need to allot 2 slots to both users. Hence we define pseudo users to redefine our problem as an assignment problem. This is explained in the figure below.

User 1	X11	X12	X21	X22
Pseudo User 1	X11	X12	X21	X22
User 2	Y11	Y12	Y21	Y22
Pseudo User 2	Y11	Y12	Y21	Y22

This matrix is now solved using the Hungarian algorithm to obtain maximum weighted matching and in turn maximize

Explosive Detector: E Nose

Neena Gilda, Guides: Prof. V Ramgopal Rao,
Prof. Maryam S Baghini and Prof. D. K. Sharma

The E Nose, an electronic replacement to sniffer dogs, is an easily operable and an economical hand held device. It can detect vapors of explosives such as TNT, RDx and about 23 other types of explosives.

Nitro based explosives are associated with their vapours in the surrounding atmosphere. This ultra-sensitive device detects these vapours, no matter how miniscule their concentration. It reports their presence even with concentrations as low as 10 few parts per trillion. A sniffer dog comes nowhere near.

The sensors used in the device have been designed and developed at the CEN lab, IITB by Dr. Seena V and Dr. Sheetal Patil. They are micro-cantilever based piezo-resistive cantilevers.

This sensor consists of multiple layers. The top layer has a strong affinity towards explosive molecules. When these molecules are in close proximity of the coating, the cantilever, which is nothing but a plank suspended at one end, is under a surface stress and bends. A piezo resistive element is embedded, which changes resistance when bent.
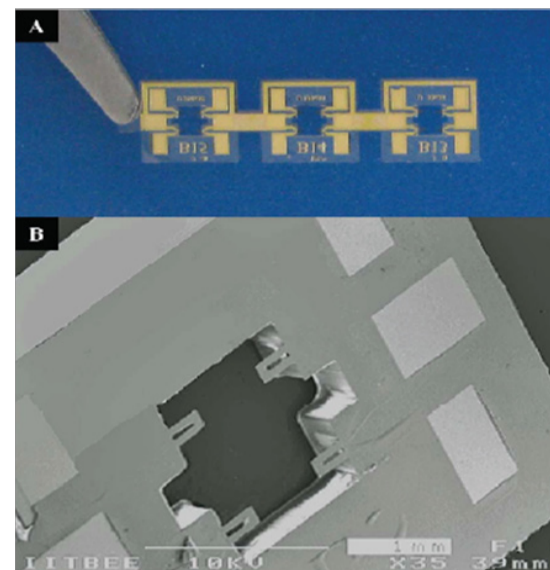
The electronic circuitry used in the device is sensitive enough to detect microscopic changes in the resistances. Initially, a traditional Wheatstone's bridge was used to get rid of thermoelectric voltages at the circuit level. However, this did not yield good sensitivity. To eliminate the errors, an ultra-sensitive circuit capable of detecting changes of over a few parts in a trillion in the resistance values was designed. In it, bi-directional constant current sources were used to actuate the modified Wheatstone's bridge. This method has been patented and was published in IEEE journals. A scholarship was granted by the CSIR, India for having presented it in two conferences at Jeju, South Korea.

The integrated sensor electronic system can be used for a wide variety of sensory applications using the current excitation technique. The chip was designed with Cadence tools with UMC 180nm scaled technology and fabricated at IMEC, Belgium. The aim is to achieve a low power sensor node integrated with wireless energy scavenging techniques.

The project was selected and demonstrated at the Techfest 2012, 2013. It was awarded the *"Gandhian Youth Technological Innovation Award"* recently.

1. **Patent for modified Wheatstone Bridge**

2. **Low power IC, designed at IIT Bombay**

3. **Gandhian Youth Technological Innovation Award**

Block Diagram

1. N. A. Gilda, S. Nag, S. Patil, M.Shojaei Baghini, D. K. Sharma and V. Ramgopal Rao, "Current Actuation Method for DeltaR Measurement in Piezo-Resistive Sensors with a 0.3 ppm Resolution", IEEE Transactions on Instrumentation & Measurement, vol. 61, no. 3, pp. 767 - 774 , Mar. 2012.
2. N. A. Gilda, S. Patil, Seena V, S. Joshi, V. Thaker, S. Thakur, Anvesha A, M. Shojaei Baghini, D. K. Sharma and V. Ramgopal Rao, "Piezoresistive 6-MNA Coated Microcantilevers with Signal Conditioning Circuits for Electronic Nose" in IEEE A-SSCC, South Korea, (Sister conference of IEEE ISSCC), pp. 121-124, Nov. 2011.
3. N. A Gilda, S. Surya, S. Joshi, V. Thaker, M. Shojaei Baghini, D. K.Sharma and V.Ramgopal Rao, "A Low-Cost, Ultra Sensitive Hand-Held System for Explosive Detection using Piezo-Resistive Micro-Cantilevers" in ISOCC, South Korea, Invited Paper, pp. 325-328, Nov. 2011.

Final handheld device with digital readout

Scanning Electron Microscope(SEM) image of the cantilevers

Giving back:
in conversation with Prof. Nair

APURV MITTAL

Professor Pradeep R Nair is one of the youngest professors and one of the more recent joining in the department. He was a Post Graduate student at IITB, as recently as 2004, and later went on to do his Ph. D at Purdue. Now he is back, as a professor, at his alma mater.
He works on Organic Transistors, LED's and Solar Cells. He also works with really small devices (NEMS) with health applications. He is interested in modelling and simulation of technologically relevant cross-disciplinary problems finding novel applications of electronic devices. He presses for collaborations with other disciplines as to produce more fruitful research, opining that these are always inspired and grounded by experimental observation that often occurs at the boundaries of multiple disciplines.

What motivated you to go for research as your career at the end of your graduation?

To answer this question, I have to go back to my college days at REC Calicut. I did a seminar on Carbon Nanotubes and this evoked an interest in me towards solid state physics. I was always excited about exploring things and device physics always appealed to me more than the circuit design. I had a job offer from Texas Instruments, but then I got admitted to IITB the same year also. I was a bit confused on which way to go. I felt that a job is a prospect which one can always go back to and coming to academics after jobs might be difficult. Education is an investment that one seldom regrets: that has been my case.

You did your PhD at Purdue. What difference did you find in the research environments at IITB and Purdue?

IITB students are not at all inferior to anyone else. This

is based my own experience as a student at Purdue and my short stay here at IITB as a faculty. Apart from the infrastructure which has been developed in any western university because of the funds being pumped from various organisations, it's the kind of problems which people solve and the way you work that makes a difference.

What do you think needs to be done to improve the research environment here at IITB?

A change to certain extent is very necessary in the viewpoint of the students. They need to be made more comfortable and confident about the research opportunities available in India as well as abroad. But the scenario has changed a lot here. Many new faculties have joined the department. A lot of infrastructure has already been developed and many more facilities are in pipeline. The productivity of the Masters/PhD students has also increased. More and more papers have gone into journal publications and I see a bright future for the institute.

What made you to come back to India after doing your PG abroad?

I had the idea of coming back to India by the time I went abroad for my higher education. I felt we needed more people working on a wide variety of problems like energy, health care and that fuelled me to come back. Also, [hopefully] the amount of impact one can make on the society might be a bit more when you are here. Also, I considered it a responsibility to come back and serve the country, where I have enjoyed many facilities starting from primary education. Personal reasons like family are definitely a reason to come back. Such and now I am a part of very exciting community over here. Its really exciting to be back where I studied.
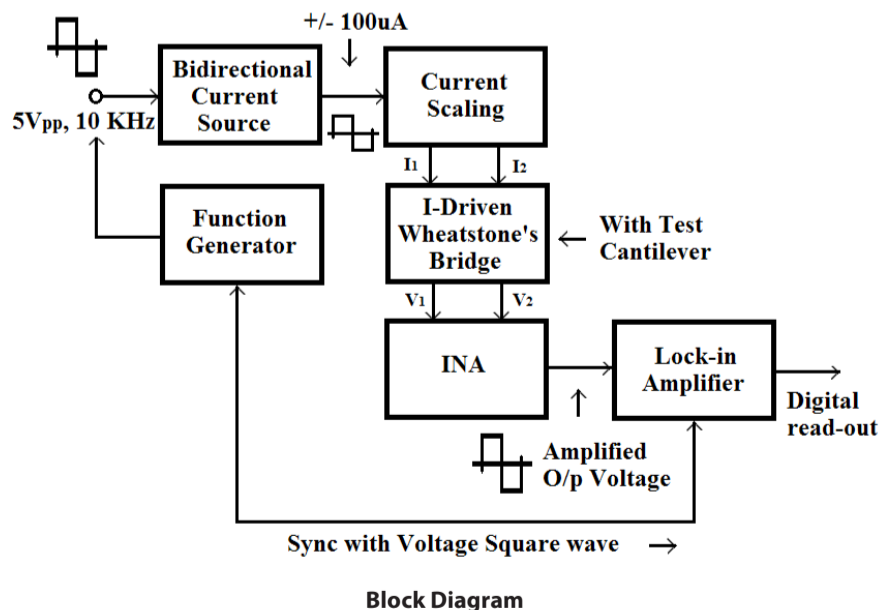
Do you have a message for the students?

To be successful in any area and especially in research, one should be
　　a) Curious about the problem you are trying to solve.
　　b) Passionate about it as if it's the problem for you to solve and not your advisor.
　　c) Put in lots of hard work and efforts along with good work ethic
Every other successful person in the history had these qualities and I think these are bare minimum for sustained excellence.

AAGOMANI

TEAM BH

Snippets from the semester gone

Aagomani, the annual department festival of Electrical Engineering, IIT Bombay, held in the first week of March last year, went almost unnoticed. Except for a few people, who were mostly part of the organizing committee of the festival, it was poorly attended and largely ignored. Scheduled for the spring semester, now is the time to retrospect, and take corrective measures.

Maharshie Yadav, normally a very enthusiastic sophomore of our department, said, "The only time I heard about the last Aagomani was at the beginning of the second semester, when a few sophomores (now thirdies) had come to visit our rooms, looking for organisers for the fest. During Aagomani, I was relaxing in my room, as the events did not look very enticing."

The event consisted of talks on radar systems and nano-electronics. There was also a tour of the nano-fabrication facility of our department, one of the best such facilities. A few workshops on Image Processing, Controls and E-Prayog were held simultaneously. Also there were three competitions – a circuit design challenge, an auto-parking bot competition and a quiz. All the events were plagued by poor participation and low enthusiasm.

Since the poor execution of this fest wastes the department and the students' time and resources, a question arises - "Why Aagomani?" Is the fest being propagated through the years only for the proliferation of PoRs, or does it serve a genuine need? What are the problems currently plaguing the fest? If there is a need, how can the fest be better? Or should it be scrapped altogether? Background Hum, in this article, serves to answer some of these questions.

Problems plaguing the fest

According to Nikhil Goyal, the Overall Coordinator of Aagomani 2012, a set of interconnected problems were present last year which led to poor execution of the fest. However, the root of the problems can be traced to the crash of the hard disk which had all the data of the previous Aagomani. "Due to some unavoidable circumstances, all the data of previous Aagomani, including that pertaining to sponsorships, was lost. Without previous data, it is tough to attract sponsors who want to know exactly what they are sponsoring."

Because of the few sponsors, the publicity of the fest was also less. This led to the fest being poorly attended by students. A possible solution was to have the department fund the fest. In response to this suggestion, Prof Abhay Karandikar replied, "We are ready to fund the festival, but provided it is held for the benefit of IITB students. Why should we fund a fest which is largely attended by outsiders?"

Another major reason for the low sponsorship were the delays in the decision making of the fest. "The lectures were finalised too late. This was a problem since the sponsors typically want to know what lecturers are coming. On the other hand, we can invite the lecturers only after getting confirmed sponsors. Also, it is very difficult to get sponsors after January, since most companies exhaust their publicity budgets in the third financial quarter itself," said Goyal.

A few suggestions

Background Hum brainstormed and came up with a few solutions. First and foremost, the fest needs to have some sort of clarity regarding its aim. Is it to bring exposure to international level talks, or is it to inculcate interest in the department among (majorly) freshmen? Also we need to look at the suggestion of professor Karandikar on department funding of the event. The fest can probably be made more interesting to the students if instead of talks by outsiders there are more low-level competitions, preceded by workshops on the same, so that even freshmen can participate.

When asked for some tips for the current organising committee, Goyal advised them to begin the work as soon as possible. He said, "It is very important that the sponsors are obtained well in time, as everything else is dependant on the sponsors." He also wished this year's team success.

> "Due to some unavoidable circumstances, all the data of previous Aagomani, including that pertaining to sponsorships, was lost. Without previous data, it is tough to attract sponsors who want to know exactly what they are sponsoring."
>
> Nikhil Goyal, OC Aagomani

Comparison with Padarth

Padarth, the Metallurgy & materials Science fest, is the antithesis of our fest, with good participation and publicity. It is scheduled to be held at about the same time as Aagomani. A slew of online events, such as photography competitions, have already taken place, while social initiatives like "Litre of Light", wherein they distributed simple chemical (bleach) light bulbs in slums, added meaning to the fest. Their quizzes, ask you about unobtainium or, Adamantium, which wolverine's bones are made of. Their Facebook page, which is being massively publicized has already gained more than 1600 followers. Their website is up and running already, and is regularly updated. In short, they connect well.

Most of their lectures and competitions are not very technical. This might actually be positive, as they can get freshmen enthused about the department rather than provide serious research talks which could be better left to more serious and respectable mediums like Institute Colloquiums.

Padarth in the print

From the Editor

Happy new year. We hope you enjoyed going through this edition of Background Hum. You must have noticed the new design, and the emphasis on readable content. Also, with the article on our department's fest, "Aagomani" this Magazine has done something it has never before - take a stand. We hope this edition of background hum has met your expectations, and that it continues to act as a great platform for showcasing talent, research while initiating debates and discussions.
We would love your feedback, on the content, as well as the design.

Sampath